Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Previously Presented) The method of Claim 23, further comprising decoding the plurality of instructions within a single clock cycle.

3. (Canceled)

4. (Previously Presented) The method of Claim 23, further comprising decoding width bits to determine the size of the instructions.

5. (Previously Presented) The method of Claim 23, where a number of simultaneous instructions is greater than 1, and further comprising communicating the number and size of the plurality of instructions to the decoder.

6. (Previously Presented) The method of Claim 23, further comprising loading a first of the plurality of instructions having a first size and a second of the plurality of

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instructions having a second size different than said first size.

7. (Original) The method of Claim 6, further comprising loading a first of the plurality of instructions having a first size, and loading a second and a third of the plurality of instructions having a second size, wherein the first size is 32-bits and the second size is 16-bits.

8. (Previously Presented) The method of Claim 23, handling the plurality of instructions within a digital signal processor.

9-22. (canceled)

23. (Previously Presented) A method, comprising:

receiving instructions from a plurality of instruction sources into a first switching part receiving size information associated with the received instructions into a second switching part;

using the first and second switching parts to switch among the instruction sources, said using simultaneously providing an instruction and associated size information at an output thereof;

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receiving the output from the first and second switching parts into a decoder; and

using the decoder to decode each instruction, using said associated size information.

24. (Previously Presented) A method as in claim 23, wherein said receiving instructions comprises receiving a plurality of instruction simultaneously and size associated with said plurality of instructions, and decoding the plurality of instructions substantially simultaneously.

25. (Currently Amended) An apparatus comprising:

a plurality of instruction sources generating instructions having varying instruction sizes;

~~a pre-decoding unit, producing instruction sizes respectively associated with said plurality of instruction sources;~~

first and second switching elements, which respectively switch instructions originating with ~~from~~ said instruction sources, and sizes of said instructions ~~from said pre-decoding unit~~, so that both said instructions and said instruction sizes are simultaneously output; and

a decoder, which receives said instructions and instruction sizes as inputs thereof.

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26. (Currently Amended) An apparatus as in claim 25, wherein said first and second switching elements switch multiple instructions to the decoder ~~at the same time said pre-decoding unit also providing an indication of a number of instructions~~, and said decoder simultaneously decodes said multiple instructions.

27. (Previously Presented) A method comprising:

producing instruction sizes respectively associated with a plurality of instructions originating from a plurality of instruction sources;

switching instructions from said instruction sources using a first switching element;

switching instruction sizes using a second switching element; and

simultaneously outputting both of said instructions and said instruction sizes to a decoder.

28. (Previously Presented) A method as in claim 27, further comprising: outputting an indication of a number of instructions concurrently with the simultaneous outputting.

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29. (Previously Presented) A method as in claim 27, further comprising: decoding the plurality of instructions within a single clock cycle.

30. (Previously Presented) A method as in claim 27, further comprising: decoding width bits to determine the size of the instructions.

31. (Previously Presented) A method as in Claim 27, further comprising: loading a first of the plurality of instructions having a first size and a second of the plurality of instructions having a second size different than said first size.

32. (Previously Presented) A method as in claim 27, further comprising: loading a first of the plurality of instructions having a first size, and loading a second and a third of the plurality of instructions having a second size, wherein the first size is 32-bits and the second size is 16-bits.

33. (Previously Presented) A method as in claim 27, further comprising: handling the plurality of instructions within a digital signal processor.

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34. (Previously Presented) An apparatus comprising:

a first switching element to receive instructions from a plurality of instruction sources;

a second switching element to receive size information associated with the received instructions, wherein the first and second switching elements are operable to switch among the plurality of instruction sources to simultaneously provide an instruction and associated size information at an output thereof; and

a decoder to receive the output from the first and second switching elements and to decode each instruction using the associated size information.

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